METHOD OF MANUFACTURING CODE ADDRESS MEMORY CELL

BACKGROUND OF THE INVENTION

Field of the Invention:

The invention relates generally to a method of manufacturing a code address memory (called CAM) cell, and more particularly to, a method of manufacturing a CAM cell by which a stack insulating film of an oxide film and a nitride film used as a dielectric film in a flash memory cell is used as a gate oxide film.

Description of the Prior Art:

A flash memory cell is used to store an ID of a manufacturing company, a serial number, and the like using a nonvolatile characteristic of a flash memory device. Also, in the flash memory device, in order to prevent deletion of information by unauthorized users, that is, in order to store protection information and un-protection information for protecting a specific memory region in which code information or the like is stored, a CAM cell circuit is inserted into a peripheral circuit region, as shown in Fig. 1.

The CAM cell used for the above purpose is generally used for repair data or protection function. Data must be easily read out from the CAM cell even at a supply power (Vcc) during a normal read operation. The CAM cell,

however, includes a flash memory cell used as a main cell.

A method of manufacturing the flash memory cell used as the CAM cell as well as the main cell will be below described by reference to Fig. 2. A tunnel oxide film **12** and a first polysilicon film **13** are first formed on a semiconductor substrate **11**. The tunnel oxide film **12** and the first polysilicon film **13** are then patterned to form a floating gate. Next, a dielectric film **14** and a second polysilicon film **15** are formed on the entire surface. At this time, an ONO film in which a first oxide film, a nitride film and a second oxide film are stacked is generally used as a dielectric film **14**. A given region from the second polysilicon film **15** to the tunnel oxide film **12** is patterned to form a stack gate in which the floating gate and a control gate are stacked. Thereafter, a source region **16** and a drain region **17** are formed on the semiconductor substrate **11** by means of impurity ion implantation process.

In the above flash memory cell, cells are programmed or erased by charging and discharging electric charges into and from the floating gate In order to perform a read-out operation for finding the program or erasure of the flash memory cell or the state of the flash memory cell, a given voltage must be applied. In other words, as shown in Fig. 3, different levels of a control gate voltage $\mathbf{V_{CG}}$, a source voltage $\mathbf{V_S}$, a substrate voltage $\mathbf{V_B}$ and a drain voltage $\mathbf{V_D}$ must be applied for respective operations of the flash memory cell.

The above flash memory cell must have a given thickness of the tunnel oxide film and the dielectric film in order to store information for about ten years. In higher-integrated next-generation semiconductor devices, it is

difficult to reduce the cell vertically. Therefore, in view of the storage capacity of the cell, it is difficult to increase the current of the cell since it is difficult to form thinly the tunnel oxide film and the dielectric film. As a result, as it is difficult to read information from the main cell using the supply power, it is a general method to read information from the cell by stepping up the gate voltage of the cell using a word line boosting circuit, etc. In case of the CAM cell located in the peripheral circuit, however, there is a problem that the area of the peripheral circuit region is increased because the CAM cell must have additional boosting circuit for this stepping voltage. Also, there is a problem that the device could not be operated without time delay because additional time for reading information is required.

Further, capacitance is generated between respective elements of this flash memory cell. In other words, there are a capacitance **Cg** between the control gate and the floating gate, a capacitance **Cs** between the floating gate and the source, a capacitance **Cb** between the floating gate and the semiconductor substrate and a capacitance **Cd** between the floating gate and the drain. In order to read out information from the flash memory cell, a coupling ratio being a capacitance **Cg** between the control gate and the floating gate to the total capacitance must be about 0.55, which lowers the conductance of the cell. Thereby, the operating voltage of the memory device used as a control gate voltage as the threshold voltage of about 2.0V same to the main cell is lowered while the cell current is abruptly reduced, which makes difficult to read given cell information. Therefore, the cell threshold voltage is lowered to abut 0V through over-erasing the cell, thus allowing

sensing of data from the CAM cell.

However, the conventional method may over-erase the cell and may thus cause a problem of storing information for a long time due to the leakage current of the cell and the like at various week operating environment such as high temperature or high voltage and the like. Further, in case of this CAM cell, if a manual test is returned to an initial state due to error when the test is performed, the conventional method has a lot of loss in time as the voltage must be lower again.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a method of manufacturing a CAM cell that is driven at a low voltage, which does not increase the area of a peripheral circuit region depending on addition of a boosting circuit and can drive the devices without delay.

Another object of the present invention is to provide a method of manufacturing a CAM cell by which an initial state need not be reinitialized and data can be stably secured when a manual test on the CAM cell is performed.

Further another object of the present invention is to provide a method of manufacturing a CAM cell capable of solving the above conventional problems by using an ONO film used as a dielectric film in a flash memory cell as a gate oxide film.

In order to accomplish the above object, a method of manufacturing a CAM cell according to the present invention, is characterized in that it

comprises the steps of forming a gate insulating film in which a plurality of oxide films and nitride films are stacked on a semiconductor substrate; forming a polysilicon film on the gate insulating film; etching given regions of the polysilicon film and the gate insulating film to form a gate; and performing impurity ion implantation process to form a source region and a drain region.

Further, a method of manufacturing a CAM cell according to the present invention is characterized in that it comprises the steps of forming a device isolation film in a given region on a semiconductor substrate to define an active region and a device isolation region; defining the active region into a cell region and a peripheral circuit region by a given process; forming a tunnel oxide film and a first polysilicon film on the entire structure and then patterning the tunnel oxide film and the first polysilicon film so that the tunnel oxide film and the first polysilicon film can only remain in a given region of the cell region, thus defining a floating gate; forming an insulating film in which the oxide film and the nitride film are stacked on the entire structure to form a second polysilicon film; patterning the second polysilicon film and the insulating film so that they can remain only in a given region of the cell region and the peripheral circuit region, thus forming a control gate in the cell region a gate in the peripheral circuit region; and performing an impurity ion implantation process for a given region of the semiconductor substrate to form a source region and a drain region, so that a flash memory cell is formed in the cell region and a code address memory cell is formed is the peripheral circuit region.

BRIEF DESCRIPTION OF THE DRAWINGS

The aforementioned aspects and other features of the present invention will be explained in the following description, taken in conjunction with the accompanying drawings, wherein:

Fig. 1 is a circuit diagram of a common CAM cell;

Fig. 2 is a cross-sectional view of a common flash memory cell that is simultaneously used as a main cell and a CAM cell;

Fig. 3 is an equivalent circuit diagram representing the capacitance of the flash memory cell; and

Fig. 4 is a cross-sectional view of a CAM cell according to the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The present invention will be described in detail by way of a preferred embodiment with reference to accompanying drawings, in which like reference numerals are used to identify the same or similar parts.

Referring now to Fig. 4, there is shown a cross-sectional view of a CAM cell according to the present invention.

A gate insulating film **22** in which an oxide film and a nitride film are stacked is formed on a semiconductor substrate **21**. For example, the gate insulating film **22** has a second oxide film **22C**, a nitride film **22B** and a first oxide film **22A**, which are sequentially stacked on the semiconductor device **21**. The gate insulating film **22** is used as a dielectric film formed between the floating gate and the control gate in the process of manufacturing a flash

memory cell. At this time, the thickness of the gate insulating film **22** is in the range of 30～300Å. For example, the gate insulating film **22** of a three layer has the first oxide film **22A**, the nitride film **22B** and the second oxide film **22C** each of which has the thickness of 10～100Å. Meanwhile, the gate insulating film **22** may be formed using a stack structure of a first oxide film, a first nitride film, a second oxide film and a second nitride film, a stack structure of the first oxide film, the first nitride film, the second oxide film, the second nitride film and the third oxide film, and the like, as well of the stack structure of the first oxide film **22A**, the nitride film **22B** and the second oxide film **22C**. Also, after forming a polysilicon film **23** on the gate insulating film **22**, the polysilicon film **23** and the gate insulating film **22** are patterned to form a gate. A source region **24** and a drain region **25** are formed on the semiconductor substrate **21** by means of impurity ion implantation process.

Though the method of manufacturing the CAM cell has been described in the above, the CAM cell can be manufactured in a portion of the peripheral circuit region when the flash memory cell is formed in a cell region in the flash memory cell manufacture process. Therefore, the process of manufacturing the CAM cell will be described in conjunction with the process of manufacturing the flash memory cell.

A device isolation film is formed on a given region of the semiconductor substrate to define an active region and a device isolation region. The active region is defined into a cell region and a peripheral circuit region by a given process. Then, a tunnel oxide film and a first polysilicon film are formed on the entire structure including the cell region and the

peripheral circuit region. Next, the first polysilicon film and the tunnel oxide film are patterned by means of lithography and etch process using a mask through a given region of the cell region is exposed. Due to this, a floating gate is defined in the cell region, and the tunnel oxide film and the first polysilicon film formed in the peripheral circuit region are completely removed. After an insulating film in which at least two or more layers of an oxide film and a nitride film are stacked is formed on the entire structure, a second polysilicon film is formed. A pattering process from the second polysilicon film to the tunnel oxide film in the cell region is performed by means of lithography process and etch process using a mask through which a portion where the floating gate in the cell region is defined and a given portion of the peripheral circuit region are exposed, thus forming a stack gate in which the floating gate and the control gate are stacked. At this time, the second polysilicon film and the stack insulating film in the peripheral circuit region are etched to form a gate. Thereafter, source and drain are formed in given regions of the cell region and the peripheral circuit region by means of impurity ion implantation process. Therefore, the flash memory cell is formed in the cell region and the CAM cell according to the present invention is formed in the peripheral circuit region. At this time, the stack insulating film is used as the dielectric film between the floating gate and the control gate in the cell region and is also used as a gate oxide film between the semiconductor substrate and the gate in the peripheral circuit region.

As can be understood from the above description, a CAM cell according to the present invention has advantages that it can be stably driven at

a low operating voltage since it uses a dielectric film of the flash memory cell as a gate oxide film. Thus, the CAM cell can reduce the area occupied by a peripheral circuit region since it does not need additional boosting circuit. Also, though the conditions for a conventional CAM cell must be reset since the CAM cell is all initialized by UV erasure when it is again tested, the CAM cell according to the present invention need not to again set the conditions on the test. Further, the present invention can secure stable data since there is nothing changes until data is artificially changed in case of once repaired data.

The present invention has been described with reference to a particular embodiment in connection with a particular application. Those having ordinary skill in the art and access to the teachings of the present invention will recognize additional modifications and applications within the scope thereof.

It is therefore intended by the appended claims to cover any and all such applications, modifications, and embodiments within the scope of the present invention.